80dB Dynamic Range 100KHz Bandwidth Inverter-based $\Sigma\Delta$ ADC for CMOS Image Sensor

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***Abstract*— A sigma delta ($\Sigma\Delta$) ADC for sensing application is presented in this paper. Several techniques are adopted to implement a low power high dynamic range ADC. Firstly, a single-stage inverter replaces the commonly used differential amplifier, in order to reduce the static current. Secondly, the normal NMOS transistor in the inverter stage is replaced by a high threshold device. As a result, with the same transistor size and supply voltage, the gain of the inverter can be enhanced while the short circuit current can be reduced. Thirdly, the charge leakage due to the forward-based parasitic diode is eliminated by using a charge protection switch and rearranged reference scheme. The proposed $\Sigma\Delta$ ADC is implemented and fabricated using TSMC 0.18μm technology. The simulation result shows that for a 1.8V supply, 25MHz sampling frequency and 125 oversampling ratio, the power consumption is 63.7μW and 116μW, dynamic range is 80dB and 83dB, the ENOB is 11.5 and 11.7bit for a single-ended and a pseudo-differential configurations, respectively. The presented ADC scheme can be applied in a Full HD image sensor running at up to 50 frames/s.**

***Index Terms*— inverter-based, $\Sigma\Delta$ ADC, high dynamic range, low power.**

I. INTRODUCTION

The continuously scaling-down trend of the device size in CMOS technology allows larger sensor array implementation on a single chip, which requires low power, moderate speed analog-to-digital converter (ADC) units. $\Sigma\Delta$ ADC is one of the most digitalized ADC schemes [1]. Normally, only the first stage integrator should be carefully designed and the amplifier is the most important analog block in the integrator. As the CMOS technology is scaling to the deep submicron feature, it is much more difficult to design the amplifier in conventional scheme [2]. Therefore, investigating a digital way to implement a $\Sigma\Delta$ ADC is important, especially when integrating the ADC within advanced system-on-chip.

Su, et al. proposed to implement the integrator of the $\Sigma\Delta$ ADC using only an inverter instead of a differential amplifier [3] and experimental results also show a significant power saving compared with the conventional $\Sigma\Delta$ ADC scheme. However, the single-ended inverter has a poor power-supply-rejection-ratio (PSRR), which can be effectively improved by using a regulated power supply, adopting a pseudo-differential configuration [4] or introducing a correlated double sampling (CDS) mechanism.

In this paper, we presents an inverter-based $\Sigma\Delta$ ADC design, featuring two major contributions. Firstly, in order to keep a 1.8V supply voltage for a large dynamic range consideration, we propose the use of high threshold voltage NMOS transistor in the inverter stage, resulting in improved inverter gain without increasing parasitic capacitance, also leading to a better linearity performance. Secondly, charge leakage due to the forward-biased parasitic diode is eliminated by using a charge protection switch scheme in the $\Sigma\Delta$ modulator design, leading to improved effect-number-of-bit (ENOB).

This paper is organized as follows. In section II, the proposed inverter-based $\Sigma\Delta$ ADC is described in detail. In section III, the simulation results are presented and compared with the previously reported designs. Section IV concludes this paper.

II. THE PROPOSED SECOND-ORDER INVERTER-BASED $\Sigma\Delta$ ADC

The block diagram of a typical second order $\Sigma\Delta$ ADC can be simplified as shown in Fig. 1.

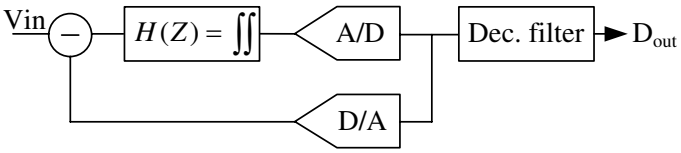

Fig. 1. Simplified block diagram of a typical second order $\Sigma\Delta$ ADC.

The most important analog circuit in this block diagram is the loop filter which typically consists of two integrators for a second-order $\Sigma\Delta$ modulator. Conventionally, the integrator is implemented by a differential amplifier with some switch capacitors. Since this differential amplifier requires large bandwidth and high slew rate determined by the sampling clock frequency, the static current consumption is very large. This large static power makes $\Sigma\Delta$ ADC less attractive compared to successive-approximation-register (SAR) ADC, in terms of the energy efficiency when ENOB is less than 12bit. Fortunately, for the second-order integrator, each amplifier does not require a high DC gain. A given ENOB defines the minimum combined gain for the second-order integrator, expressed in Eq. 1 [6].

$$ENOB \leq \log_2\left(\frac{VREF}{\Delta V_{IN}}\right) \approx \log_2\left(Av_1 \cdot Av_2\right) + C \qquad (1)$$

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Where, the value of C depends on the cap ration $C1/C2$ and for a 12bit ENOB, the combined gain $Av_1 \cdot Av_2$ is in the order of 72dB, referring to a 100 gain for each inverter with an 8dB margin. In order to address this energy efficiency issue, some low-power high-speed integrator with low static current schemes were proposed such as VCO-based integrator [5] and inverter-based integrator is the simplest amongst them. Generally, an inverter-based integrator uses an inverter as the amplifier. Without a virtual ground, the offset voltage of the inverter should be auto-zero and stored in a capacitor during the reset phase. During the charge transfer phase, the inverter performs as a class AB or class C amplifier [4]. The DC gain for a typical CMOS inverter can be derived as follows.

$$\begin{aligned} &A_v = (g_{mN} + g_{mP})(r_{oN} // r_{oP}) \\ &\begin{cases} g_m \propto V_{gs} - V_{th} \\ r_o \propto \frac{1}{\lambda (V_{gs} - V_{th})^2} \end{cases} \end{aligned} \tag{2}$$

It is clear that the gain is approximately inversely proportional to the overdrive voltage ($V_{gs} - V_{th}$). Choosing a proper supply voltage, the inverter can achieve a good trade-off between power consumption, gain and speed [7]. However, for a large dynamic range requirement, it is not desirable to degrade the supply voltage, which is KT/C limited.

Instead of achieving a high-gain low-power inverter by tuning the supply voltage [7], in our design we replace the normal NMOS transistor in the inverter by a high threshold voltage device (using a 3.3V NMOS transistor). The DC gains and the slew rate of the proposed and normal inverters as a function of the supply voltage are shown in Fig. 2, for a 300fF load capacitance. The slew rates for both inverter schemes are similar by tuning the transistor size. The gain of the proposed inverter is however larger than the normal inverter across the supply voltage range from 1V to 1.8V. In other words, if increasing the gain of a normal inverter to the same value as the proposed scheme by supplying a lower Vdd, its settling time will be lower than the proposed inverter. As a result, a high gain and large slew rate inverter is achieved with a low parasitic capacitance and 1.8V power supply, leading to a high dynamic range ADC performance.

Another issue is the charge leakage. Conventionally, the capacitor C_2 is directly connected to the output of the inverter [4]. This connection may introduce a forward-biased parasitic diffusion diode in the switch transistor S_{CP}. As a result, the charge in this diode will leak to the supply or ground. A transient simulation is performed in Fig. 4. A, indicating this charge leakage phenomenon. The forward-biasing only happens when the floating voltage is beyond Vdd or Gnd after turning off the charge transfer switch S_{CT}. We use an additional switch S_{CP} as a charge protector, as shown in Fig. 3. In the design [3], S_{CT} is used only for the consideration of reducing clock feed-through. The auto-zero mechanism in [3] is also different from our design. We use a dedicated capacitor C_{AZ} to store the offset voltage, instead of storing it using C1, where $C_{AZ} = 4C1$. Since $C2 = 4C1$, the total capacitance for the proposed integrator is only $9C1$, compared to a twice

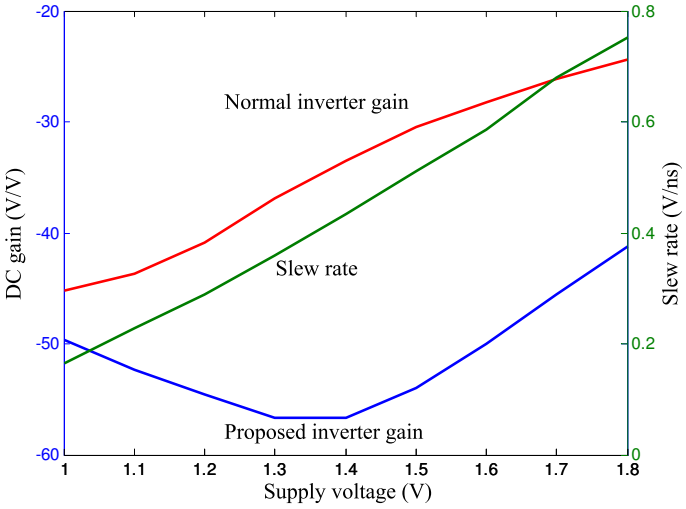

Fig. 2. Simulation results for the gain and slew rate as a function of the supply voltage on the conditions of 300fF load capacitance for the normal inverter and the proposed inverter.

larger capacitance in [3] and thus, both power consumption and chip area are reduced.

For the similar consideration in terms of charge leakage, we connect node A to a reference voltage of about 0.6V, instead of connecting to Gnd as reported in [7]. Shown in Fig. 4. B, there is no forward-biasing state at the NMOS transistor's diffusion region. Therefore, the charge leakage is eliminated. It should be noted that, for a pseudo-differential configuration, these techniques mentioned above are also effective.

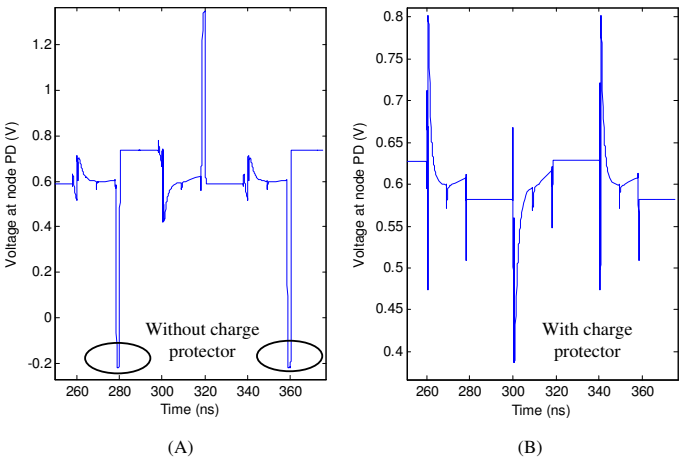

Fig. 4. Transient simulation for the voltage in the diffusion parasitic diode without (A) and with the rearranged switches and references (B).

The ratio of C1/C2 is 1/2 which performs a trade-off between noise shaping efficiency, the inverter's output swing and chip area, according to the signal-to-noise-and-distortion-ratio (SNDR) simulation result. The sampling capacitance C1 is only 75fF since the KT/C noise is reduced by multiple sampling, which can be much smaller than a conventional Nyquist ADC's pF level sampling capacitance [7].

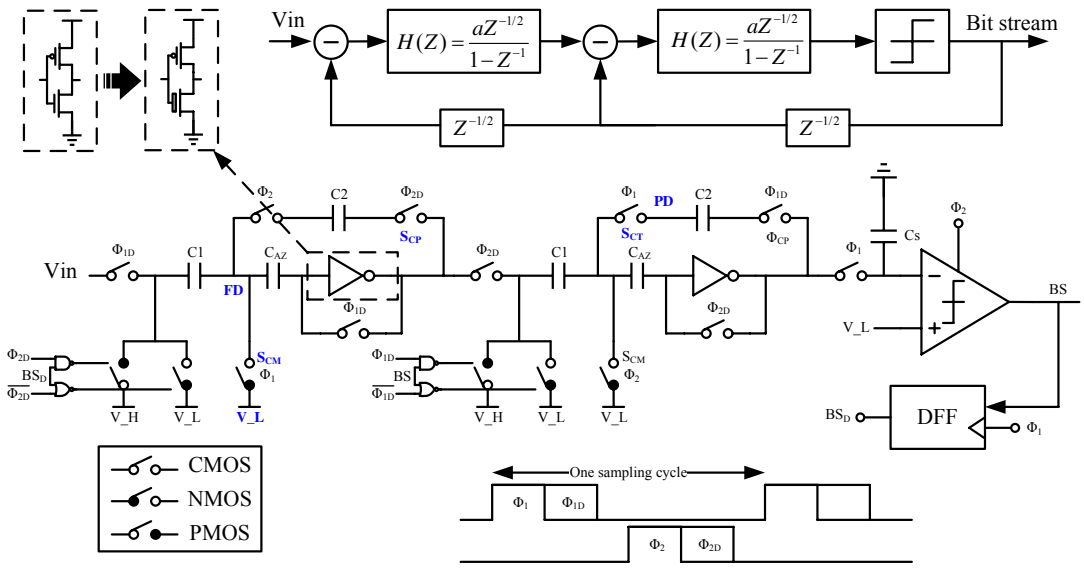

Fig. 3. The proposed inverter-based sigma delta ADC schematic.

III. Chip Implementation and Simulation

The proposed inverter-based ΣΔ ADC with a single-ended and pseudo-differential configurations are implemented using TSMC 0.18μm mixed-signal 1p6m technology. The quantizer is implemented using a dynamic latch. D flip-flop is used for the delay element. Fig. 5 shows the layout of the modulator part. The layout has only 7μm pitch in order to meet the requirement for a CMOS image sensor pixel feature. A free run is simulated and 12500 points bitstream is recorded for each result. As shown in Fig. 6, the dynamic ranges of the proposed ADC are 80dB and 83dB, the peak values of SNDR are 72.7dB and 73dB (11.79bit and 11.84bit ENOB) under 25MHz sampling clock and 125 oversampling ratio, for a single-ended and differential configurations, respectively. The bandwidth is 100KHz which is a basic requirement for a column-parallel ADC array, implemented in a Full HD (19201080) resolution image sensor running at 50 frames/s. The power spectrum density with a 20kHz -9.5dB sinusoid input voltage is shown in Fig. 7, indicating a second-order noise shaping. The linearity of the proposed ADC is shown in Fig. 8, with a second order 12b decimation filter and 125 sampling cycles. With DC voltage inputs, the peak INL is +/-10LSB (+/-0.25%) while DNL is limited to +/-0.1LSB (+/-0.0025%). The performance of the designed chip is summarized in Table I.

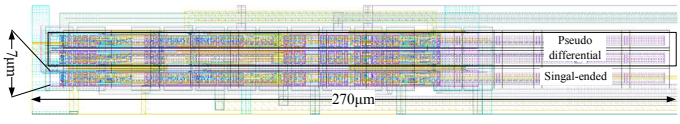

Fig. 5. Layout of the ΣΔ modulator.

In order to compare the proposed ADC with other previously reported work, two Figure-of-Merits about energy efficiency (FOM_1) and chip area efficiency (FOM_2) are defined by

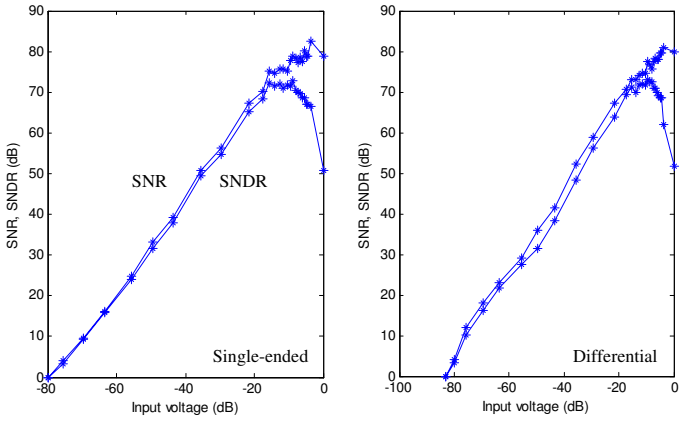

Fig. 6. The simulated SNR and SNDR as a function of the input amplitude for a single-ended (A) and a pseudo-differential (B) configurations.

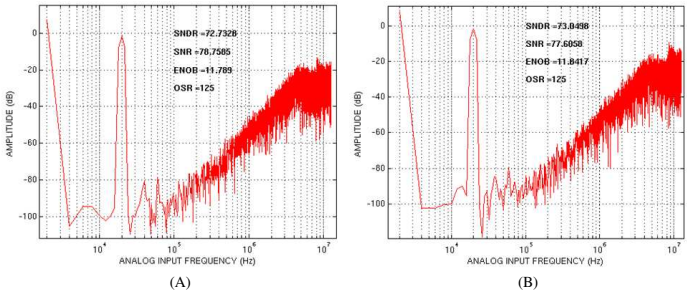

Fig. 7. The simulated power spectrum density for the single-ended (A) and differential ADC (B) for a 20kHz -9.5dB sinusoid input.

TABLE II

FIGURE-OF-MERITS COMPARISON

Specification	This work Single-ended Δ	This work Pseudo-differential Δ	[3] Δ	[3] *	[4] *	[4] *
Power consumption	63.7μW	116μW	40μW	42μW	36μW	5.6μW
Core area	1890μm^2	3780μm^2	540200μm^2		715000μm^2	3024μm^2
Order	2	2	3	3	3	2
Peak SNDR	72.7dB	73dB	69.01dB	61.96dB	81dB	63dB
ENOB	11.79bits	11.84bits	11.17bits	10bits	13.16bits	10.17bits
Bandwidth	100KHz		20KHz			8KHz
Process	0.18μm					0.35μm
FOM1	88.5fJ/step	159fJ/step	434fJ/step	1000fJ/step	98fJ/step	300fJ/step
FOM2	2.36 e-6 μm^2/step.Hz	4.56e-6 μm^2/step.Hz	5.9e-3 μm^2/step.Hz	13.2e-3 μm^2/step.Hz	1.9e-3 μm^2/step.Hz	1.64e-4 μm^2/step.Hz

Δ Simulation results

* Measurement results

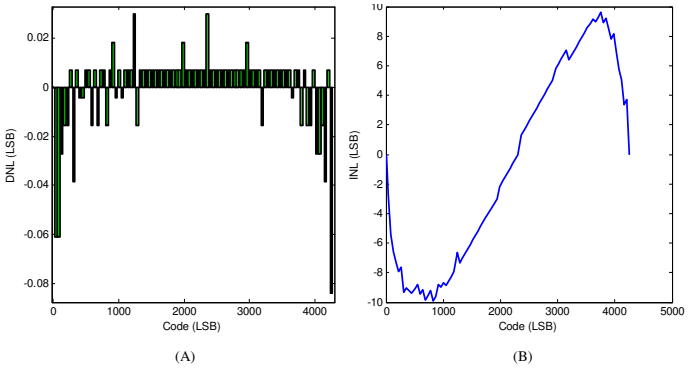

Fig. 8. Simulated Differential Non-linearity, DNL (A) and Integral Non-Linearity, INL (B).

TABLE I

CHIP RESULT SUMMARY

Specification	Single-ended	Pseudo-differential
Dynamic Range	80dB	83dB
Peak SNR	80dB	81dB
Peak SNDR	72.7dB	73dB
Power consumption	63.7μW	116μW
Core Size	270 x 7μm^2	270 x 14μm^2
Signal Bandwidth	100KHz	
Sampling Frequency	25MHz	
Supply Voltage	1.8V	
Technology	TSMC 0.18μm mixed-signal 1p6m	

Eq. 3 and Eq. 4, respectively [7]. The comparison results are summarized in TABLE. II, showing obvious improvements for both criterions.

$$FOM_1 = \frac{Power}{2^{ENOB} \times 2 \times BW} \tag{3}$$

$$FOM_2 = \frac{Area}{2^{ENOB} \times 2 \times BW} \tag{4}$$

IV. CONCLUSION

A second-order ΣΔ ADC is presented in this paper. In the proposed design, the integrator is implemented by using an inverter, which has a normal threshold PMOS and a high threshold NMOS transistors. As a result, without sizing up the transistors and losing dynamic range, the proposed inverter can achieve a large DC gain with high dynamic range. Additionally, the charge leakage due to the forward-based parasitic diode is eliminated by using a charge protection switch and rearranged reference scheme. Simulation results using TSMC 0.18μm process show that using a 1.8V supply voltage, 25MHz sampling frequency and 125 oversampling ratio, the power consumptions are 63.7μW and 116μW, the peak SNDRs are 72.7dB and 73dB, the dynamic ranges are 80dB and 83dB, for a single-ended and pseudo-differential configurations, respectively.

ACKNOWLEDGMENT

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